Design Software Integrates Synthesis, Simulation and Optimization for Complete Design Automation

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According to TechWeb's online encyclopedia (techencyclopedia), Electronic Design Automation (EDA) means "using the computer to design, lay out, verify and simulate the performance of electronic circuits on a chip or printed circuit board." [1] The term EDA has been loosely applied to a number of different sets of software programs that address (and sometimes actually automate) various stages of the design cycle. Sometimes EDA is used to mean schematic entry and simulation while at other times it has been used to refer to schematic capture and layout software.

Before computers were widely available, circuits were drawn by hand on drafting boards using mechanical drafting tools. Eventually, computer-aided design (CAD) software became available for creating schematics using large mainframes and minicomputers and computer-aided engineering (CAE) was used to analyze the designs. However, prior to the advent of the personal computer, the cost of computing forced many designers to do circuit design and layout manually. Almost immediately after the introduction of the personal computer, affordable circuit design software began to appear. In the mid-1980s, all the CAD and CAE tools for electronic circuits coalesced into the term "electronic design automation." [1]

Drafting circuit schematics by hand was a slow process, so when this task could finally be accomplished by a computer the software that automated this task was considered design automation software. RF and microwave circuit design software has come a long way since then, so we should expect a lot more from EDA software than simply automated schematic drafting or even circuit simulation. Circuit simulation, verification and physical layout represent the back end of the design process. A great deal of advancement has been made in software that addresses the front end of the design process- i.e. in circuit synthesis software.

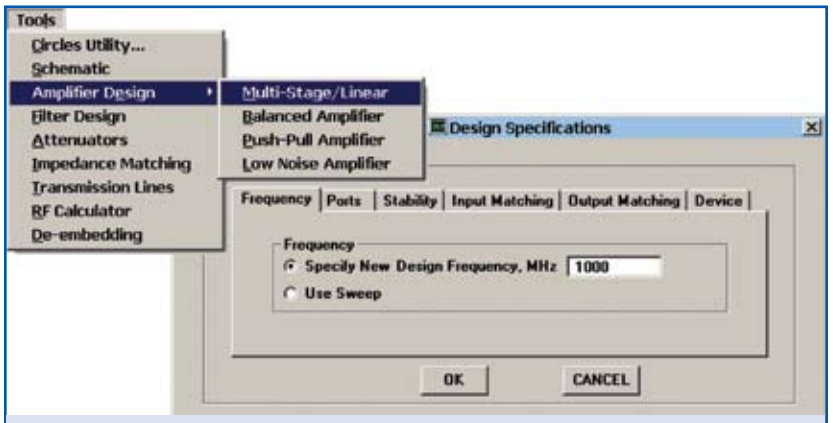

Figure 1

This article will show how the new LINC2 design automation software from ACS can help the designer 1) create the initial circuit design from a set of design requirements, 2) analyze the circuit with a circuit simulator, 3) optimize the circuit, and finally 4) verify that the circuit can perform as required when component values vary over their full tolerance ranges.

Circuit Synthesis

Circuit synthesis programs can provide the highest level of design automation because they can take design specifications as input from the designer and automatically produce a schematic that captures the design requirements. Sometimes software is sold as EDA software even though it does not contain true automatic synthesis capability. When the software package does not include automatic circuit synthesis it is like the computer-aided design or computer-aided engineering software of the past, in that it functions as an aid to the design process but doesn't automatically perform the actual design.

The LINC2 design suite has a comprehensive set of circuit synthesis modules for automating the design of lumped and distributed filters, single and multi-stage amplifiers, low noise amplifiers (LNAs) as well as a number of other devices and circuit components. Because impedance matching is so fundamental to the successful performance of RF and microwave circuits, LINC2 includes a synthesis package devoted entirely to the design of impedance matching networks.

This full-featured synthesis tool recognizes the modern trend for RF circuits to commonly employ balanced topologies that interconnect with RF ICs (integrated circuits) with differential ports. Thus, the LINC2 matching network tool synthesizes balanced matching networks as well as balun circuits for transforming between balanced and unbalanced circuits while simultaneously providing the required impedance match. Even the LINC2 attenuator design tool can synthesize balanced and unbalanced attenuators for equal or unequal terminations. The LINC2 amplifier design package also provides the option of incorporating the balanced topology into amplifier synthesis. LINC2 Amp Pro can design amplifiers with balanced ports for stand-alone push-pull operation or for direct insertion between differential circuits.

Previous articles in this magazine outlined the complete design flow, employing EDA from circuit synthesis, simulation and verification to physical layout using LINC2 filter synthesis examples [2] [3]. Using EDA to make complex tradeoffs between a number of competing design parameters was illustrated in the October 2005 MPD article "Unique Software Tool Automates the Design of Low Noise Amplifiers" [4] and in "A Design Tool for Improving the Input Match of Low Noise Amplifiers" from the February 2007 issue of High Frequency Electronics [5].

An emerging trend in RF circuit design for wireless communications is the need for broadband circuits to support high data rates with complex wideband modulation schemes. In the following design example exact circuit synthesis will be used to generate an initial two stage amplifier circuit capable of producing the maximum available gain from both transistors at the center of a specified frequency band (1000 MHz in this example). The LINC2 optimizer will then be employed to flatten the frequency response to produce a broadband amplifier with 26.5 (+/- 0.75) dB gain over the 100% bandwidth from 500 MHz to 1500 MHz.

Wideband Amplifier Synthesis Design Example

The design goal for this example will be to design a two stage linear amplifier with 26.5 dB gain over a 100% bandwidth from 500 MHz to 1500 MHz. The gain should be at least 25 dB but no more than 27.5 dB (for a 2.5 dB peak-to-peak gain ripple) over the entire band. The output return loss should be at least 10 dB over 75% of the (upper) band and great than 7.5 dB over the remainder of the band. The design will be implemented in microstrip with 5% (+/- 2.5 %) tolerance on dimensions.

LINC2 amplifier synthesis is started by selecting Amplifier Design > Multi-Stage/Linear from the Tools menu. This action pops up the Design Specifications Form as shown in **Figure 1**. The Design Specifications Form allows the user to control the details of various aspects of the design. The user can specify the frequency, port impedances, stability criteria, topology and type of input and output matching network (such as whether to use lumped or distributed networks), device selection and the inter-stage matching network if a multi-stage design is selected.

For this example 1000 MHz is entered for the center of the operating frequency band. The

default values for port impedances (50 ohms) are accepted. The defaults for stability considerations are also accepted. In this case the devices are unconditionally stable at the design frequency. However, if the active device selected was potentially unstable, then this tool can direct the program to automatically stabilize the device in the circuit synthesis.

Distributed networks are selected for the input and output matching networks as shown in Figure 2. Series and shunt transmission lines (TRL-Stub), quarter wave lines, or stepped-impedance transmission lines (TRL Transformers) are among the options that can be specified. In this example, the choice is to use the Stub-TRL method.

Enabling Select topology at run-time provides more control over the design by allowing for more details about a particular topology to be specified during the synthesis process. Otherwise, if this option is not checked, the program will automatically use certain defaults for any additional parameters relating to a particular network topology.

Finally, the Device tab is used to select the number and type of devices used in the design. In this example, two devices are selected (a BFR520 and an NE02135 NPN transistor) so Device Inter-stage Matching options appear below the devices in Figure 3. Clicking on the inter-stage matching option box opens up a list of up to nine different inter-stage matching methods. Here, the ¼ Wave line was selected to match the output of the first device to the input of the second device. Clicking OK at this point starts the amplifier synthesis.

Options for the device inter-stage matching appear as shown in Figure 4. Here, lumped or distributed elements in series or shunt orientation can be applied at the device terminals to cancel the device reactances. A 75 ohm shorted stub was used at the output of the first device and a 65 ohm open stub was applied to the input of the second device. A 90° (1/4 wave) line matches the resistances (real parts of the device impedances). Specifying details of the inter-stage matching network is optional since the program can be directed to automatically synthesize the inter-stage matching without prompting the user for input. Clicking OK to accept the inter-stage matching topology automatically generates the schematic for the two stage amplifier shown in Figure 5.

Optimizing for Broadband Response

The impedance and electrical length of the series transmission line elements in the schematic (Figure 5) can be selected for optimization. Only the length of the shunt elements need to be optimized because the impedance they present to the circuit is a function of their length.

The optimizer is set up for exactly 26.5 dB gain (M21 = Magnitude[S21] = 26.5 dB). The output return loss is set for a minimum of 15 dB (M22 = Magnitude[S22] < -15 dB). The input return loss is intentionally not specified so that it can vary in a way that will flatten the gain response. A typical optimization specification for this design is shown in Figure 6.

LINC2 analysis indicates that the maximum available gain for both of the active devices in cascade is 26.33 dB at the maximum operating frequency. Therefore, the second gain optimization goal was set for at least 26.33 dB at 1500 MHz and given a weight of 5 to help counter the gain roll-off at the high end of the band. After optimizer is finished, the new element values are automatically updated in the schematic by selecting Update Schematic or Update & Exit from the Optimizer's File menu. The optimized schematic is shown

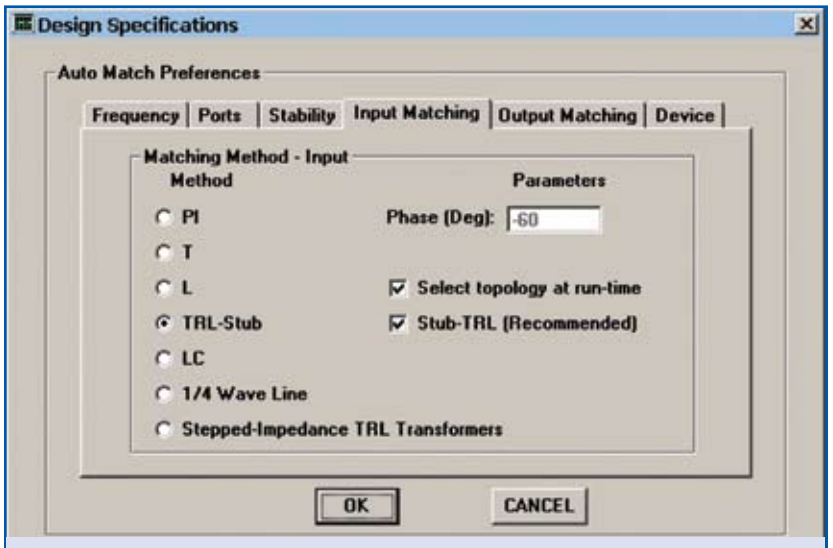

Figure 2

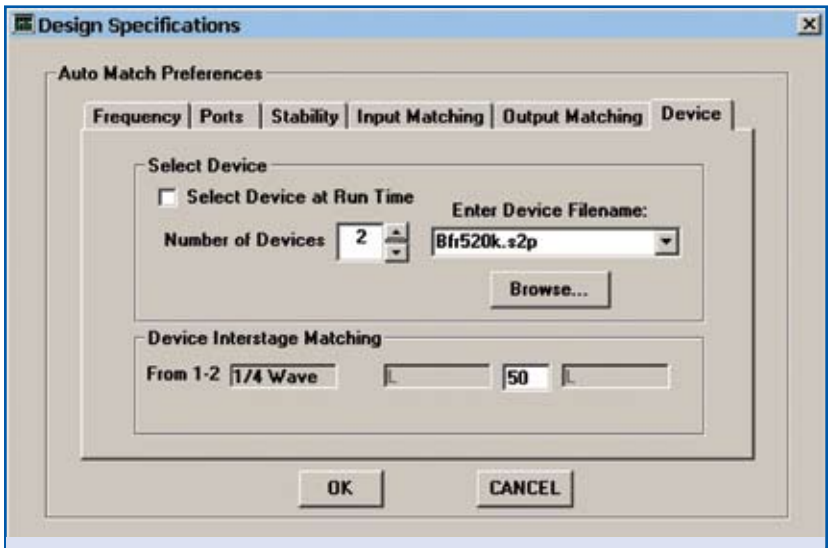

Figure 3

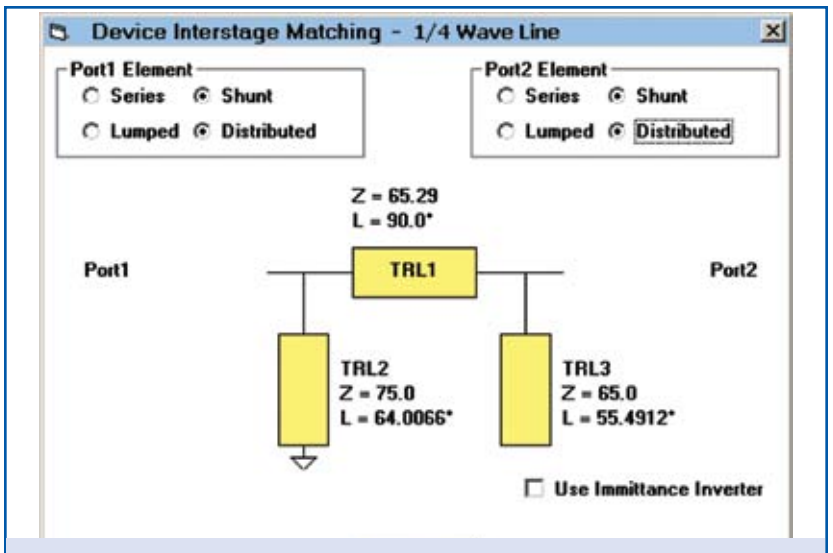

Figure 4

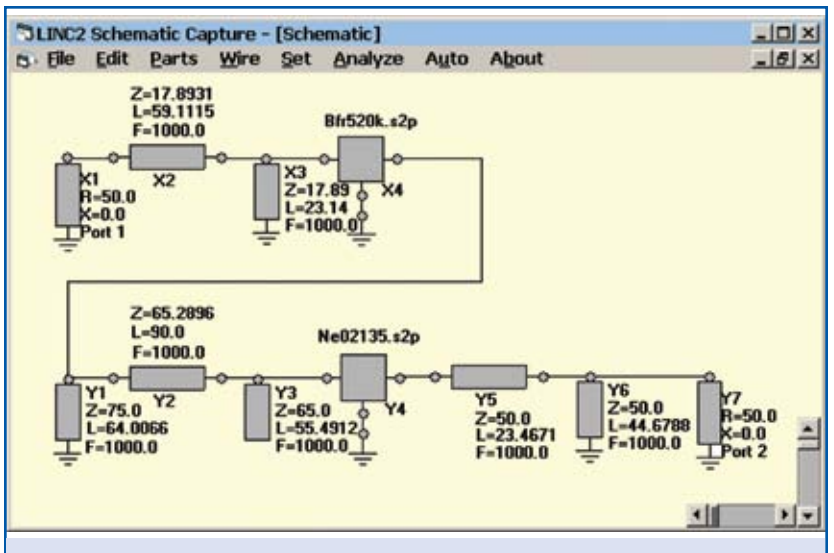

Figure 5

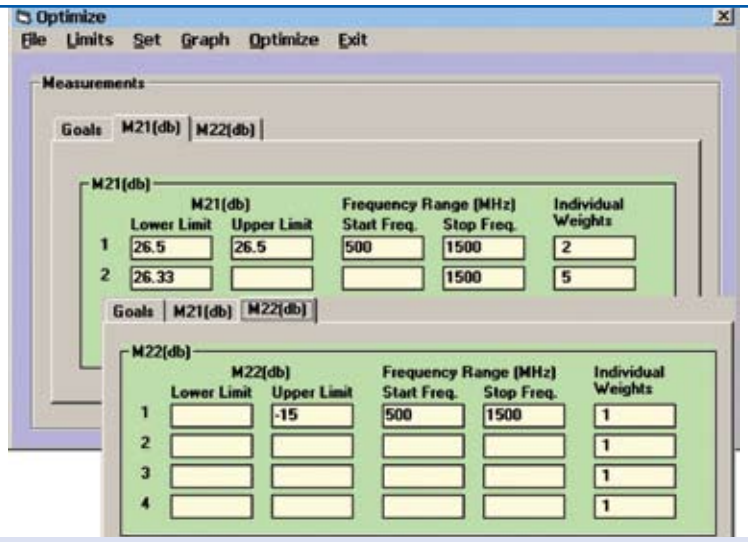

Figure 6

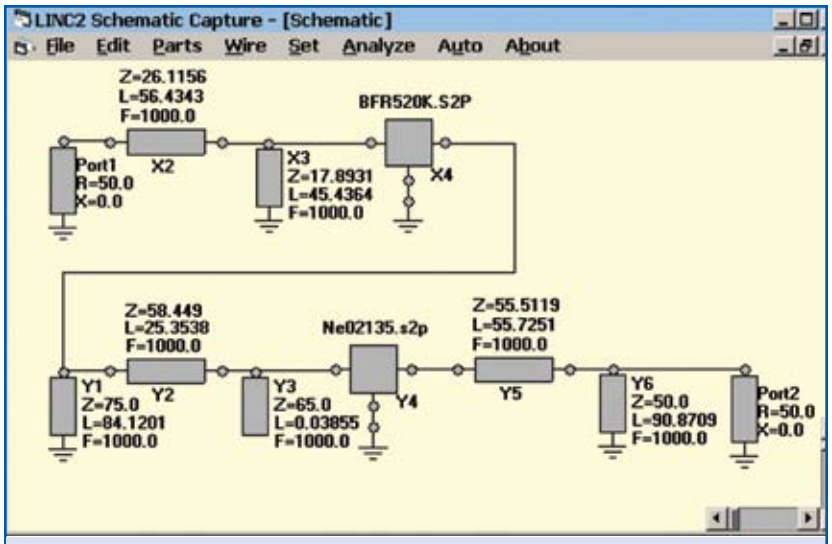

Figure 7

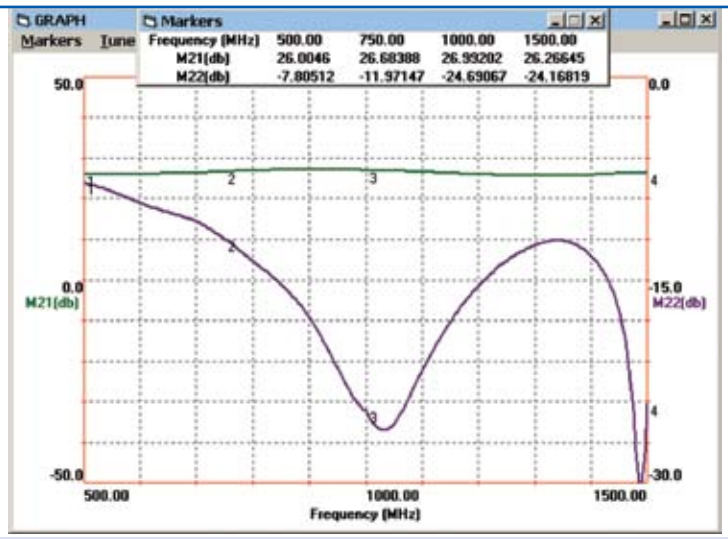

Figure 8

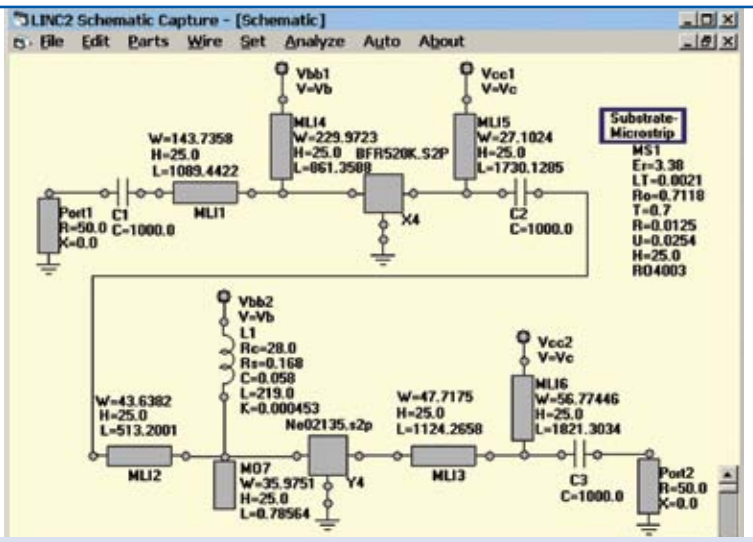

Figure 9

in Figure 7.

The simulation results for the optimized amplifier circuit are shown in Figure 8. The amplifier has a 1 dB bandwidth in excess of 1000 MHz centered at 1 GHz (> 100% bandwidth). The gain response is flat at 26.5 dB with less than 1.5 dB peak-to-peak ripple over the entire 1000 MHz band.

So far the design is still in the synthesis stage where all circuit elements are ideal electrical transmission line models. LINC2 automates the process of converting all of the transmission line models in the schematic to physical microstrip or stripline. With one menu pick (Auto | Convert T-Lines To…| Microstrip) all the electrical schematic elements in the optimized schematic of Figure 7 are immediately converted to their physical equivalents as shown in Figure 9. In the schematic of Figure 9, 1000 pF DC blocking capacitors and a choke for supplying DC bias to the base of the second transistor have been added. The shorted stubs have all been utilized as DC feeds to bias the transistors.

Circuit simulation

In a matter of seconds the ideal optimized circuit has bee transformed into a schematic rendering all the essential dimensions required to construct the physical prototype (all dimensions in Figure 9 are in mils). The important point to be considered now is how much performance has been lost in the conversion to microstrip. This question can be answered by running a circuit simulation on the schematic in Figure 9. Selecting Analyze from the menu bar in the schematic window produces the results shown in Figure 10.

In Figure 10 the responses for gain and output return loss are displayed as grey plots for the microstrip amplifier circuit. The responses for the circuit using ideal transmission lines are overlaid as green (gain) and purple (output return loss) traces. The plots for the optimized transmission line circuit are so nearly identical to those of the microstrip circuit that they mostly cover the grey (microstrip) plots. Above the graph in Figure 10 are marker readouts giving numerical data for gain (M21) and return loss (M22) at 250 MHz intervals across the band. The marker data at the top represents the transmission line data while the marker block just below it shows the data for the microstrip version. Comparing the data for the ideal and physical circuits indicates that very little performance change occurred after converting to microstrip. The use of very low loss circuit board material and accurate microstrip synthesis were responsible for the excellent results in which there was less than 0.4 dB difference in gain and 1.5 dB difference in return loss across the band.

Circuit Performance Verification

LINC2 statistical yield analysis employs Monte Carlo simulations to determine the likely yield for a large number of samples. The goals for the desired outcome are entered as shown in Figure 11. Minimum values, maximum values or both can be entered for any design goal, and the frequency range over which the goal applies can be specified.

All components selected for tuning or optimization are listed in the Tolerances menu. The default tolerance is +/- 5%, but each component parameter can be selected individually from the menu and its tolerance can be changed to any other value. The tolerance value for all components can be set to any range by selecting Reset Tolerances from the Set menu. In this example, the range for all microstrip dimensions (length and width) are set to +/- 2.5% for a total dimensional tolerance range of 5%.

Clicking Calculate Yield performs the yield analysis over the specified number of samples. In this case the sample size was set to 2000. Yields for the individual goals are dis-

played next to the goal while the total yield is displayed at the bottom of the statistics window. The total yield shows the number of successful results over the total number of trials performed. The percentage of successful trials is also displayed. Checking Show Graph in the Graph menu displays the results for each trial run graphically as shown in Figure 12.

For the microstrip amplifier circuit of Figure 9, the yield is 100% for gain variation, 100 % for the 10 dB return loss specification and 97.5% for the 7.5 dB return loss spec.

Summary and Conclusions

A design procedure in which circuit synthesis is used to create the initial circuit for subsequent analysis and optimization was presented. A two stage wideband amplifier circuit designed using the LINC2 program demonstrated that virtually complete design automation can be realized when design software integrates circuit synthesis with schematic capture, simulation, optimization and design verification.

Though not included within the scope of this article, the speed and efficiency at which circuit synthesis software can be employed to test a variety of "what if" scenarios should be obvious to the reader. For example, the amplifier design in this article utilized only one of many available distributed input/output matching topologies. However, would the broadband characteristics of ¼ wave stepped-impedance transmission line transformers have enabled greater bandwidth or better return loss over the given band? Or, would a lumped multi-element solution have provided a better match considering the relatively low (500 MHz) frequency at the low end of the band? The answer to these and many other questions can be answered in a matter of seconds with circuit synthesis. The synthesis program automatically creates the circuit schematic and sets up the simulation environment ready for simulation, so the results are immediate.

LINC2 is a high performance, low cost, RF and microwave design and simulation program that includes many value added features for automating design tasks, including circuit synthesis. More information about LINC2 can be found on the ACS web site at www.applied-microwave.com.

References

[1] http://www.techweb.com/encyclopedia.

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[3] Henkes, Dale D., "New Filter Synthesis Software Designs Space Efficient Interdigital Filters", Microwave Product Digest magazine, June 2007.

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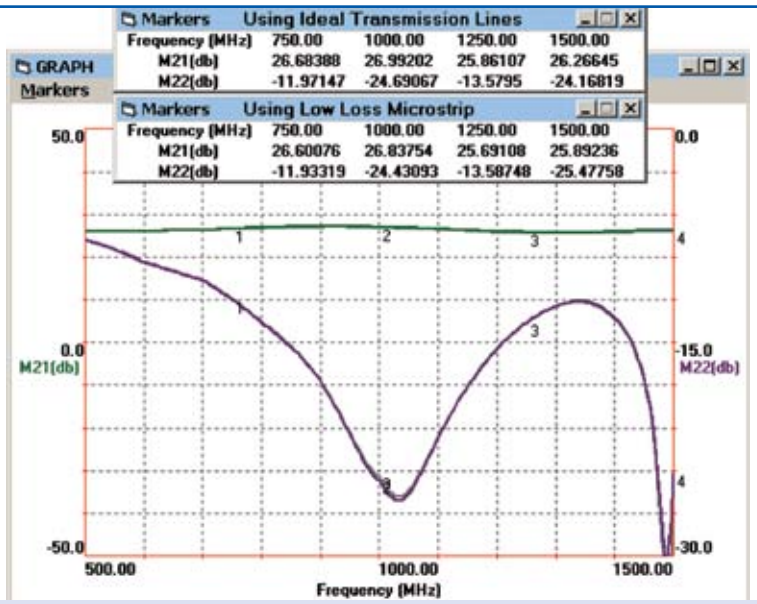

Figure 10

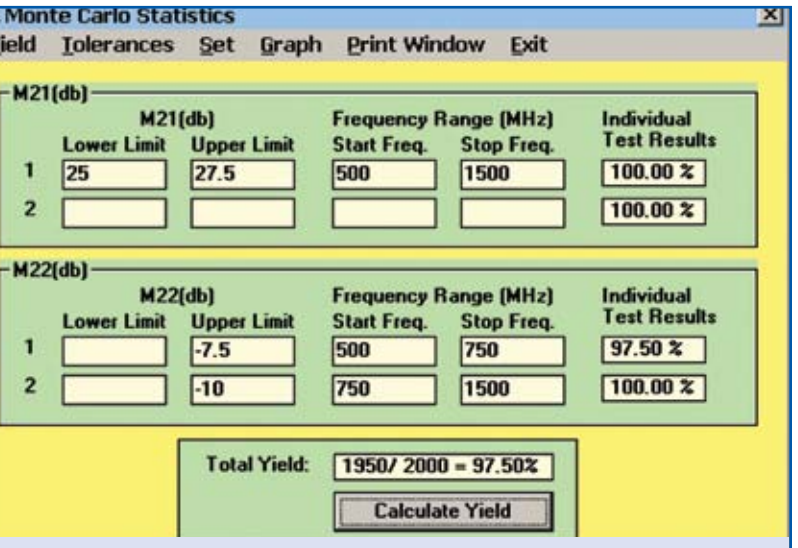

Figure 11

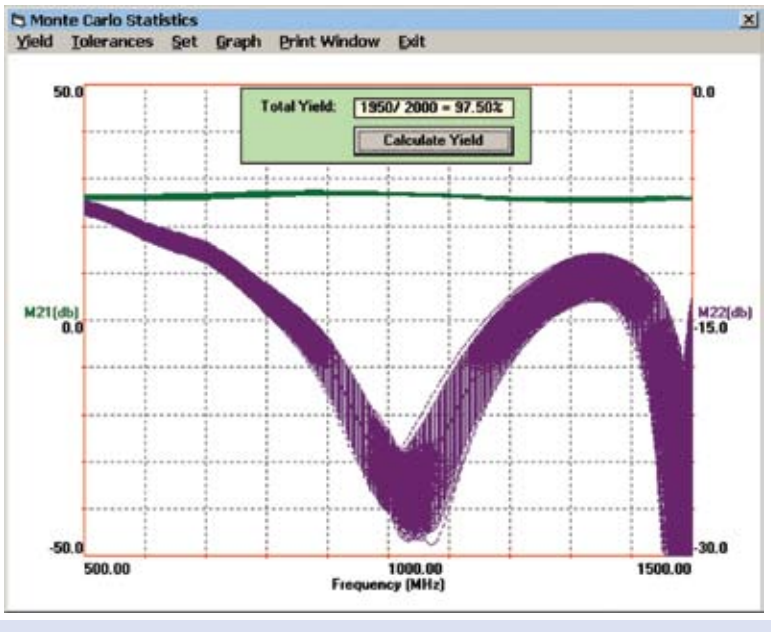

Figure 12