LINC2 Synthesis, Optimization and Yield Analysis – Three Key Components for Successful First Pass Circuit Design

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As the use of high frequency simulation software became indispensable to the task of designing modern RF and microwave circuits, most EDA (Electronic Design Automation) software packages that addressed this market included at least two core ingredients; circuit simulation and circuit optimization based on a numerical optimizer. These two software tools became so ubiquitous that design methodologies coalesced around their combined use. However, circuit simulation is strictly analysis, not design. Moreover, an optimizer can only make adjustments to the component values of a circuit topology that is already known. It cannot, on its own, come up with a more optimum circuit topology. Although RF and microwave circuit designers exhibit great skill in the application of these tools, the fact that they are often used to "design" circuits even though neither is capable of circuit synthesis has lead to certain undesirable consequences.

First and foremost, circuit design via the simulation/optimization cycle is a trial and error process with no guarantee of success. There are a host of reasons why an optimizer may fail to bring a particular circuit design into compliance with the desired design goals. The process relies heavily on the ability of the practitioner to select a viable circuit topology from a library of pre-existing circuit designs or past experience. The likelihood of successfully designing a circuit by simulation/optimization is directly proportional to the degree that the circuit (and initial component values) presented to the optimizer resembles the desired circuit, i.e. optimization works best when the answer is already known! [1]

For example, it is generally known and accepted that changing the specifications for a filter design may force a change in the filter topology, requiring at least an increase in filter order (increasing the number of components) or a completely new filter type (a radical change in topology) in order to meet the new or improved performance specifications. Most designers would not attempt the futility of trying to use an optimizer to tweak the filter's component values in order to meet a new set of specifications that are substantially more demanding. And yet, for active circuit design, there are practitioners who would attempt to optimize the input and output matching networks of an existing amplifier circuit in order to match to a new device or transistor. One example of where this attempt might fail is if either of the matching networks use one of the eight possible configurations of the common two-element L network. All attempts to optimize the component values to reproduce a match to the new device will fail if the impedance of the new device lies outside the reach of the particular L configuration used. Only a change in topology, such as using a different L network, will solve the problem. Unfortunately, the designer may not realize the futility of the effort until a great deal of time has been spent with the optimizer.

Another problem that can arise with the simulation/optimization procedure is that the optimizer can get stuck in a local minimum in the error function. When this happens, the user is left without any clear idea of how to proceed. Should different weights and constraints be placed on variables? Is a different circuit topology required, or simply a different set of initial component values?

To help eliminate these problems, a design procedure is outlined in Figure 1 that includes synthesis, simulation, and yield analysis. Optimization is included in the design process flow when needed to compensate for the inclusion of parasitic elements or when ideal components are replaced by physical models. For narrowband designs, the synthesis program can produce circuit prototypes that are exact and optimization used near the end of the design process (Figure 1) is performing the role of fine tuning (mostly to account for

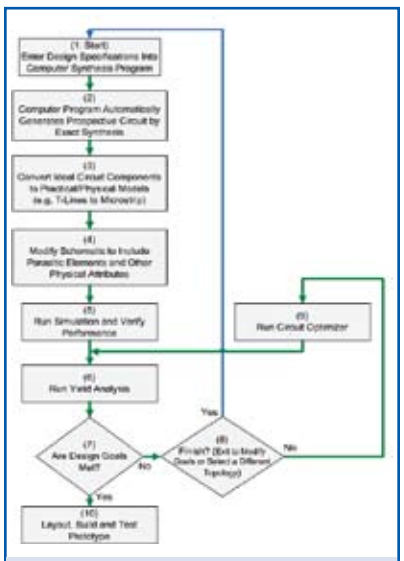

Figure 1: The Design Flow

Figure 2: Stability Section of the LINC2 Design Specification Form

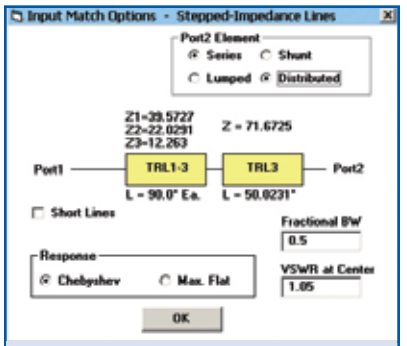

Figure 3: LINC2 Input Match Details

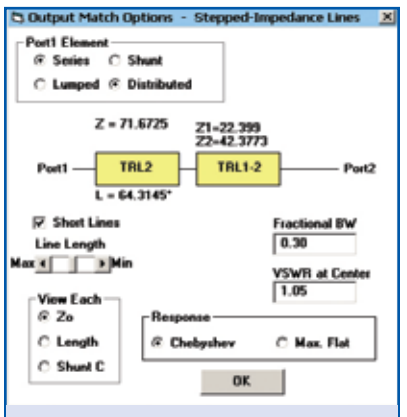

Figure 4: LINC2 Output Match Details

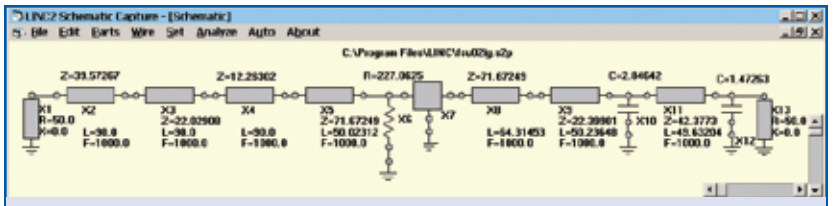

Figure 5: LINC2 Synthesized Amplifier Schematic

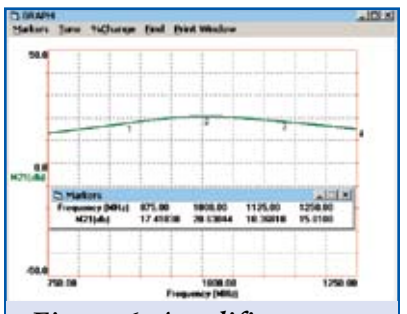

Figure 6: Amplifier Frequency Response (Initial Synthesized Circuit)

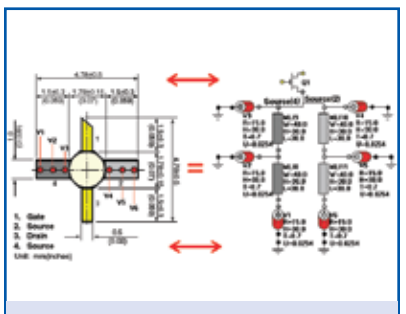

Figure 7: FET Source Grounding with Multiple Ground Vias

slight performance shifts due to parasitics). In this case the optimizer has virtually a 100% chance of meeting the goals if they are in line with the original synthesis specifications. In the case of wideband design where an exact solution may not be available, the synthesis program can generate an approximate solution or one that meets some specification over a portion of the frequency band (allowing the optimizer to attempt to finish the job of bringing the design to compliance). Even in wideband design where the optimizer is more heavily used, it still benefits greatly from circuit synthesis seeding it with an approximate solution.

Not all optimizers are alike. Some compromise speed for accuracy while others leave it up to the user to figure out (by trial and error process) which type of optimizer is best suited for the problem at hand. The advanced LINC2 optimizer, provided as an integral part of the LINC2 software suite, is powerful, easy to use, and adaptive, thus taking the guesswork out of employing the right type of optimizer. Another reason for using the LINC2 optimizer is that it provides additional capability that may not be found in other optimizers. For example, the new LINC2 optimizer accepts user defined equations that provide additional control over the optimizer above and beyond the usual circuit response goals. The following amplifier design example will demonstrate how the LINC2 optimizer can take into account an equation that formulates a (user specified) constraint on the physical size of the circuit (e.g. the total length of all microstrip used in the design).

Having the ability to optimize equations is a very powerful tool because it gives the designer control over the outcome of the design in ways that are not necessarily related to electrical performance, and yet may be just as important as the electrical (circuit response) performance. Thus in LINC2, the physical dimensions are one example of an aspect of the design that can be optimized along with the electrical performance. Then lastly, yield analysis provides a final check that the desired performance holds up when component values are allowed to vary over their specified tolerance range.

Therefore, the key to successful first pass circuit design includes circuit synthesis, optimization, and yield analysis in conjunction with simulation. The LINC2 Pro software suite from ACS (Applied Computational Sciences) includes all of these essential program modules. LINC2 integrates filter synthesis, amplifier synthesis (including LNA design and synthesis), matching network synthesis, and component synthesis with a high performance circuit simulator. This article will use these essential LINC2 program features to demonstrate the design flow of Figure 1.

LINC2 Amplifier Design Example

In the following example, LINC2 will be used to design a GaAs FET linear amplifier for 17 db gain from 750 to 1250 MHz, for a 50% bandwidth centered at 1000 MHz. It is desired that the gain variation should not be more than +/- 0.5 dB across the band. Also, it will be a further design goal to match the output of the amplifier to a 50 ohm load with a minimum of 10 dB of return loss everywhere throughout the 750 to 1250 MHz band. The design processes shown in Figure 1 will follow sequentially.

1. Start with Circuit Synthesis

Design flow processes 1 and 2 (Figure 1)

In Designing Microwave Circuits by Exact Synthesis [1], Minnis states that exact synthesis "can be applied to almost any microwave circuit or component, including those containing active devices. [Exact circuit synthesis offers] the opportunity to build new circuits from scratch from a selection of basic circuit elements. There is no dependency on existing circuit structures and there are few restrictions on network topology… Unlike any process based on numerical optimization, synthesis is guaranteed to find a valid network solution for a given target performance specification, whatever the nature of the specification." With this endorsement and the comments above on the problems associated with the non-synthesis (simulation/optimization) approach, it is obvious that it is a good idea to start circuit design using synthesis whenever it is available.

Exact Circuit Synthesis

The broad definition of the word synthesize, meaning to create, needs to be narrowed to reflect the specific meaning used here. The meaning

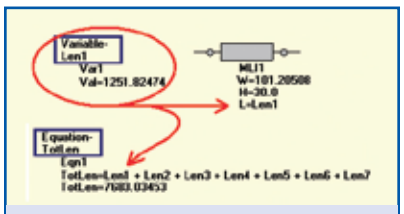

Figure 8: Creating and Using a LINC2 Variable

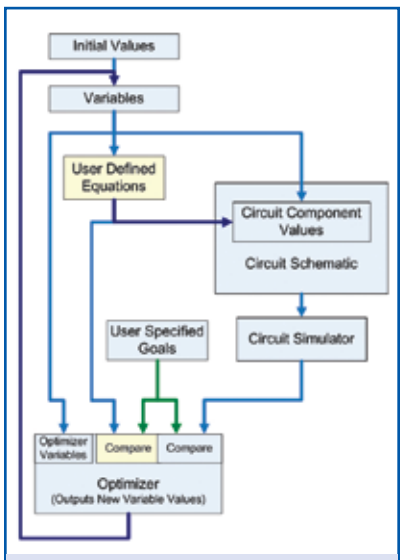

Figure 9: Including User Defined Equations in LINC2 Optimization

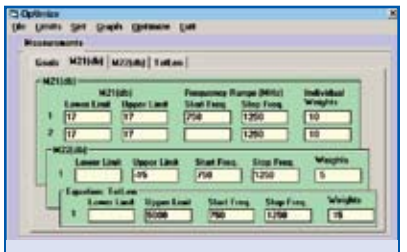

Figure 10: Setting LINC2 Optimizer Goals and Weights

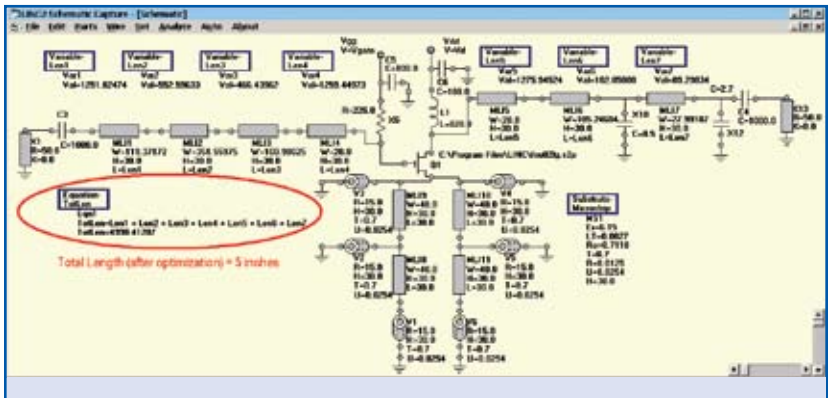

Figure 11: Final LINC2 Optimized Amplifier

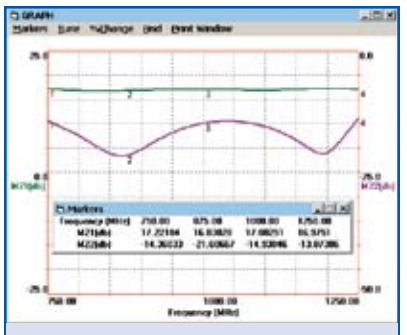

Figure 12: LINC2 Optimized Gain and Return Loss

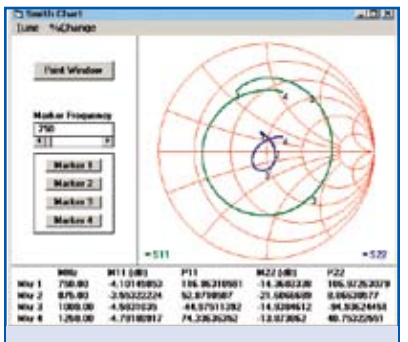

Figure 13: LINC2 Optimized S22 (S11 not Optimized)

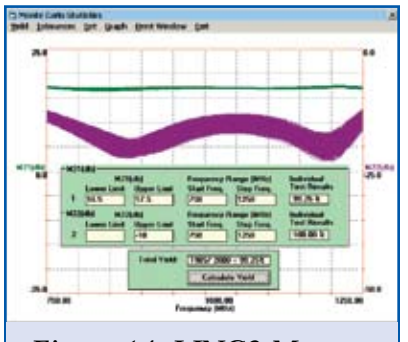

Figure 14: LINC2 Monte Carlo Simulations (2000 samples)

of exact circuit synthesis here is a computer program that employs an algorithm and/or a set of mathematical equations or functions for the purpose of directly mapping a set of design specifications into a circuit schematic that will meet the specifications. Moreover, the circuit element values are computed by mathematical functions or algorithms and not by a numerical optimizer. The results are immediate since there is no optimization loop and the usual long delays that are associated with its iterative nature.

Amplifier synthesis for this example starts by selecting Amplifier Design > Multi-Stage/ Linear from the LINC2 **Tools** menu. This action pops up the Design Specifications Form as shown in Figure 2. The Design Specifications Form allows the user to control the details of various aspects of the design. The user can specify the frequency, port impedances, stability control, topology and type of input and output matching network (such as whether to use lumped or distributed networks), device selection and the inter-stage matching network(s) if a multi-stage design is selected. Figure 2 shows the LINC2 Design Specifications Form with selections from the Stability Tab displayed. LINC2 can automatically stabilize an unstable device when synthesizing a circuit. This process is completely automated and does not require any input from the user. However, the Stability section is available (by clicking on the Stability Tab) should the user want certain control over the process and its methods.

As with the Stability Tab, design options made available by clicking the Input Matching and Output Matching Tabs are optional. If not selected, default matching networks will be provided. For this example, Stepped-Impedance transformers are selected for the input and output matching networks and "Select Topology at Run-Time" is also checked for finer control over the implementation details of the matching networks. Full quarter-wave stepped-impedance transmission line transformers are selected for the input network (Figure 3) while shortened (< _ Wave) lines are chosen for the output (as shown in Figure 4). The input matching network is comprised of a number of quarter-wave line sections in a cascade of impedance steps designed to match impedances over a broad bandwidth. As shown in Figure 4 for the output network, LINC2 has the unique ability to arbitrarily shorten the length of the lines and thus compress the size of the network as requested by the user. The trade-off over the full length (1/4 wave or 90 degree) lines is reduced matching bandwidth as the length of each line section is reduced.

Finally, clicking the Device tab brings up a file browser for selecting the type of device(s) that will be used in the design. For this example, the Eudyna FSU02 GaAs FET was selected for the active device. Clicking **Synthesize** and choosing the network details (Figure 3 and 4) automatically synthesizes the LINC2 amplifier schematic shown in Figure 5. The schematic in Figure 5 represents the RF elements of the amplifier circuit including ideal components with exact values. A circuit simulation can now be run to determine the degree to which the circuit thus synthesized approaches the desired design goals.

The frequency response (Figure 6) for the initial synthesized amplifier circuit shows good potential for meeting the design goal of 17 db across a 50% bandwidth centered at 1000 MHz. Indeed, the gain response yields more than 17 dB over most of the band with greater than 20 dB of gain at the center.

2. Convert Ideal Elements to Physical Models

Design flow process 3 (Figure 1) The next step is to convert all the ideal transmission line models in the (synthesized) schematic (Figure 5) to physical microstrip. LINC2 automates this process entirely. With one menu pick (**Auto > Convert T-Lines To...> Microstrip**) all of the electrical schematic elements in the schematic of Figure 5 are immediately converted to their physical equivalents as shown in Figure 11. Every ideal line (described by characteristic impedance, electrical length in degrees, and frequency) has been replaced by an equivalent physical microstrip line (described by trace width, length, and height of the supporting dielectric substrate). Anyone who has used a transmission line calculator to go through a schematic and manually convert all of the electrical (ideal modeled) transmission lines to physical lines will appreciate the way LINC2 automates this process.

In the schematic of Figure 11, LINC2 automatically derived microstrip lines MLI1 through MLI7 from the seven ideal transmission lines in schematic 5. Table 1 shows the length and width values generated by the initial synthesis. The table also shows the length and width of these line after unconstrained and constrained optimization (discussed later in the following sections).

3. Add Physical and Parasitic Elements Not Included in Synthesis

Design flow process 4 (Figure 1) Microstrip lines MLI8 through MLI11 were added to represent the source leads of Q1. The details of the FET's source via structure is shown in Figure 7. Figure 7 relates a pictorial [2] of the FET's physical package and lead structure to the equivalent area in the amplifier schematic. The six vias (V1 - V6) shown in red in the schematic portion to the right side of Figure 7 correspond to the six red circles placed (equally spaced) along the two source leads of the packaged part on the left side of the figure (representing the physical locations of the ground vias). The left source lead (MLI8

Table 1: Component Values - Synthesis and Optimization; Unconstrained and Constrained

Matching Network		Input Network				Output Network			Total Line Length
Component (Microstrip)		MLI1	MLI2	MLI3	MLI4	MLI5	MLI6	MLI7	
Initial Synthesis -	Length (mils)	1378.8	1321.2	1276.3	802.7	1032	738.3	764.5	7313.8
	Width (mils)	64.3	149.6	308.1	20	20	146.4	57.4	
Unconstrained Optimization -	Length (mils)	1251.8	1293.2	1207	1254.8	1297.8	734.4	644	7683
	Width (mils)	101.2	235	111	20	20	82	24.9	
Optimization Constrained with **Total Length Equation (TotLen)** -	Length (mils)	1251.8	552.6	466.4	1259.5	1275.9	102.9	89.3	4998.4
	Width (mils)	119.4	351.6	160.9	20	20	105.2	28	

and MLI9 in the schematic) is shown in dark grey while the right source lead (MLI10 and MLI11) is shown in light grey. Each source lead trace is divided into two microstrip sections in the schematic to accommodate the placement of the ground vias. (The gate and drain leads are shown in yellow in Figure 7).

The 227 ohm stability resistor at the gate of Q1 (Figure 5) has been utilized as a gate supply feed in Figure 11 (where its value has been changed to the nearest standard value of 226 ohms). Other elements required to couple DC and RF power to the circuit include the following: C3 and C4 couple RF in and out of the amplifier respectively while blocking DC. Bypass capacitors C5 and C6 are applied at the gate and drain supply feeds (Vgg and Vdd) while choke L1 is used to feed the drain supply to Q1. All of these changes are part of design flow process 4 in Figure 1, i.e. the process of modifying the schematic to capture parasitic elements and other physical attributes. If appropriate care is taken, these physical elements can be added in such a way as to minimize the effect on circuit performance.

4. Run a Circuit Simulation to Verify Performance

Design flow process 5 (Figure 1)

A simulation run on the circuit in Figure 5 ***after converting to physical (microstrip) lines*** reveals that only 0.6 dB of gain was lost (worst case) across the band compared to the original synthesized circuit in Figure 5. This represents the difference between lossless (ideal) and lossy (practical) lines in this frequency band. Should the addition of parasitic and physical elements significantly affect the circuit response, then optimization can usually restore the performance. Figure 6 indicates that optimization will be needed to flatten the gain response to 17 dB over the desired band.

One final point should be noted before going on to the section on optimization. The FET has four leads that must be accommodated by microstrip traces that should be at least as long and wide as those of the packaged part. That is the reason why MLI8 through MLI11 were added to the synthesized schematic. MLI8 and MLI9 together equal the length and width of the left source lead. Similarly, MLI10 and MLI11 together accommodate the right source lead. Multiple ground vias along these microstrip traces ensure that the source of the FET is adequately grounded.

Since the synthesis program provided only an electrical ground *symbol* at the FET's source (location X7 in Figure 5), any kind of ground structure that adequately represents an ideal ground is acceptable. Therefore, the structure shown connected to the source of Q1 in Figure 11 was constructed with the correct combination of ground vias for good grounding and traces sized to absorb the device leads. The gate and drain leads also must be physically accommodated by traces that are large enough to absorb the leads when the part is mounted and soldered down to the circuit board. However, unlike the source leads, who's affects can be removed from the circuit with ground vias, the gate and drain leads are in series with the signal path and will directly become part of the input and output matching networks.

Using an optimizer to alter the rest of the matching network in an attempt to remove the effects of the gate and drain leads is often the design procedure employed for dealing with this issue. As discussed earlier in this article, it is likely that this procedure will fail. However, close observation of Figure 11 reveals that the gate and drain leads have already been accommodated by properly sized microstrip traces. Figure 7 indicates that the device's gate and drain leads are each 59 mils long and 20 mils wide. It is interesting to note that the microstrip connected to the gate and also the drain microstrip (MLI4 and MLI5 respectively in Figure 11) are both exactly 20 mils wide as required, and more than long enough to fully absorb the device leads. But how did this very fortunate situation come about given that these lines are both part of matching networks that were automatically created by the LINC2 synthesis program? The answer attests to the power and versatility of LINC2 synthesis.

The versatility of LINC2 synthesis lies in the many opportunities it provides for the designer to guide the design. The user can choose how much control one has over the details of the LINC2 synthesis process. For example, the LINC2 amplifier synthesis module can automatically design a single-stage, or even a multi-stage amplifier, for maximum gain with only the frequency and the device(s) specified by the user. On the other hand, the design example in this article employed choices available on the Design Specifications Form that led to more detailed control over the design of the matching networks.

After selecting Stepped-Impedance TRL Transformers for the basic matching topology, checking the option box "Select Topology at Run-time" causes the synthesis program to pop up windows for selecting additional matching options as shown in Figures 3 and 4. These additional options for Stepped-Impedance Lines allow the user to control the bandwidth and target VSWR (quality of match), the shape of the matching frequency response (Chebyshev or Maximally Flat), and the choice of type and orientation (lumped or distributed in shunt or series orientation) of an additional element for canceling the load reactance. It was this option of being able to select an additional series distributed element that enabled the circuit synthesis program to include a TRL (transmission line) on the gate and drain sides of the matching networks that would accommodate the device leads. The ability to edit the impedance of the additional series TRL to any value supplied by the user allowed for making it exactly 71.6725 ohms. This is the value indicated by the LINC2 transmission line calculator for 20 mil wide microstrip on the specified circuit board material (for 30 mil thick substrate with Er = 6.15). Thus, the user was able to guide the program toward producing matching networks with microstrip traces that perfectly accommodate the device leads-all by direct synthesis without the trial and error involved with using an optimizer.

5. Optimization

Design flow process 9 (Figure 1)

In narrowband amplifier design exact circuit synthesis is more likely to achieve the design goals over the desired (but relatively small) frequency band. In this case, the design would proceed (after circuit synthesis) through design flow procedures 5, 6, 7, and 10 as shown in Figure 1. That is, it may be possible to bypass the optimization process if parasitic and physical elements have not disturbed circuit performance too much.

For wideband design, it may be the case that exact circuit synthesis can no longer directly produce a circuit meeting the performance goals over the entire band. It was pointed out that the simulation results displayed in Figure 6 do not meet the design goal of 17 dB gain over the desired band. Therefore, optimization will be required to flatten the gain response to 17 dB.

The LINC2 optimizer is enabled by checking the **Tune** option box for each component parameter that will be optimized. For the initial optimization run, the values of the two capacitors in the output network and the widths and lengths of all the microstrip traces were included in the list of components to be optimized (except MLI4 and MLI5 which need to remain at a width of 20 mils for the device leads). Before optimizing the circuit in Figure 11, the total length

of all microstrip from input to output (MLI1 through MLI7) was 7.3 inches (see Table 1, Initial Synthesis). When the optimizer finished the gain was 17.0 +/- 0.25 dB over the entire band and the worst case output return loss was 12.25 dB with nearly 15 dB of return loss over most of the band. Thus, the design goals were met but the total length of microstrip (MLI1 through MLI7) increased to nearly 7.7 inches. Table 1 shows that the length of these microstrip lines had grown to a total of nearly 7.7 inches after unconstrained optimization.

During optimization the total line length grew to 7.7 inches because the optimizer was not limited in the range over which it could adjust the variables or component values. Most optimizers (including LINC2) allow constraints to be placed on variables or circuit component values that are to be optimized. The LINC2 optimizer allows constraints in the form of boundaries (the optimized value must lie between some lower and upper limit) or as a percentage (+/- %) of the initial (nominal) value. Thus, the increase in line length could have been prevented by restricting each line to an upper limit no large than its original (pre-optimized) value. However, this places unwarranted restrictions on the optimizer since some lines may need to be lengthened while others would produce best results by being shortened. Unfortunately, the user has no way of knowing the best way to constrain the line lengths and still provide the optimizer with the necessary freedom to find a solution that meets the design goals.

What is needed is a global goal, such as **total line length**, that can be constrained during optimization while the individual line lengths are unrestrained. User defined equations can be added to the list of optimizer goals with the new LINC2 optimizer, making this capability a reality for the first time in version 2.72. The next section will show how the new LINC2 optimizer can optimize an equation formulated to equal the total length of all seven microstrip lines (that make up the input and output matching networks). The equation can be optimized to meet a certain goal (such as reducing the overall line length by 35%). It is a powerful new capability that these user defined equations can be optimized right along with circuit performance goals, even though the equation is not necessarily related to the electrical performance of the circuit.

Optimizing Circuit Performance Using Unconstrained Optimization

A LINC2 schematic, like the one shown in Figure 5, can be optimized for circuit responses meeting the stated performance goals as is, without creating named variables. The value of a component parameter can be included in the list of parameters to optimize by simply double right clicking the mouse over the part to be optimized and then checking the **Tune** box next to the parameter to be included in tuning or optimization. The widths of mircostrip lines and the values of the capacitors in the schematic were selected for optimization this way. However, as shown in Figures 11, the length of microstrip lines are defined by variables (Len1 through Len7) so that an equation can be written that keeps track of the total line length as follows.

As shown in Figure 8, a named variable can be assigned to a circuit component parameter or it can be included as a variable in a user defined equation, or both. Figure 8 shows how the value of variable Len1 becomes the length parameter for microstrip MLI1 as well as the first length variable in the equation TotLen (Eqn1). In Figure 11, variables are set up above each microstrip line who's length will be controlled by the corresponding variable. Equation TotLen captures the total length of these lines. After running an unconstrained optimization on the synthesized schematic involving the length variables, selected line widths and the capacitor values, the results are displayed in Table 1. (See **Unconstrained Optimization** in Table 1 for the optimized component values). As mentioned earlier, the goals for gain, gain flatness and return loss have all been met while the unconstrained optimized length of the lines total 7.68 inches.

An Optimizer for Equations and Circuit Performance

Figure 9 shows the workings of the new LINC2 optimizer with its ability to optimize user defined equations along with the usual circuit responses. In the usual process, variables are created, assigned to certain circuit component parameters and sent to the optimizer as inputs (optimization variables) to be adjusted in a closed loop process that compares circuit responses with desired user specified goals. In the new LINC2 program, these same variables can also be included as variables in an equation (or number of equations) defined by the user. The equation(s) can formulate the variables into simple or complex mathematical expressions. LINC2 equations can combine variables using simple arithmetic or they can include math functions such as exponential, trigonometric or logarithmic functions (including functions that call other functions). In this example, simple addition is used to add up all the line lengths.

After an equation has been written and placed on the schematic its value can be assigned to a circuit component parameter by name. The same equation value, referenced by the equation's name, can be included as one of the goals for the optimizer. Figure 10 shows how the optimizer's goals and weights are set up for this example. Equation TotLen is included along with the magnitudes of S21 and S22 (M21 (dB) and M22 (dB) respectively). The gain goal for S21 is exactly 17 dB while the goal for output return loss (M22) is 15 dB in an attempt to acquire margin against the actual stated goal of 10 dB minimum across the band. And finally, the goal for the total line length equation, TotLen, was set at 5000 (mils) for a 35% reduction in length over the previously (unconstrained) optimized value of 7683 (mils).

Figure 11 shows the final optimized schematic indicating that a total line length just under 5 inches has been achieved in the optimization process. Figures 12 and 13 report that all the other design goals have also been met. The gain is 17 dB flat over the entire operating band with less than 0.5 dB peak-to-peak ripple. The output return loss is approximately 14 dB or better over the band. S11 was not a goal and so it was not optimized. It is possible that S11 could be improved by including it in the optimizer goals. The low input return loss could also be mitigated by placing an isolator at the amplifier's input or by placing two identical amplifiers in a balanced configuration between 90 degree hybrid couplers.

6. Yield Analysis

Design flow process 6 (Figure 1)

A Monte Carlo Yield analysis was run on the final optimized circuit in Figure 11. The results are shown in Figure 14 for a sample size of 2000 random variations in component values uniformly distributed over a tolerance band of +/- 5% for lumped components and +/- 2.5% for distributed (microstrip) elements. At 100% for output return loss and 99.25% for gain, the yield is very good given these tolerances. When the tolerances are tightened to +/- 2% for all components the yield is a solid 100% for both gain and return loss goals.

When exact component values have been replaced by the nearest standard values and all significant parastics, physical models and practical circuit details (such as ground vias, bias chokes, bypass and DC

blocking capacitors etc.) have been taken into account and the circuit still passes the yield analysis test, then it is time to move on to the final process (**design flow process 10** in Figure 1), i.e. layout, build and test the physical prototype. This completes the amplifier design example.

Summary and Conclusions

A design process was presented that includes synthesis, simulation, optimization and yield analysis. The process outlined in Figure 1 offers an alternative to the "design by simulation/optimization" cycle. The alternative design method employs circuit synthesis software to produce a prospective circuit design that includes a working topology with computed component values that are exact. In the case where optimization is necessary to tune out the effects of added parasitics (and other practical circuit details), the optimizer may still benefit from a circuit synthesis program seeding it with an initial circuit, complete with component values that are already well along in the process of meeting the design requirements.

This approach was demonstrated by using the LINC2 software suite from ACS to design a microwave amplifier for flat gain response and good output return loss over a 50% bandwidth centered at 1 GHz. Size considerations allowed for only a moderate amount of design and analysis detail. For example, the addition of models for capturing parasitic elements was mentioned but stepped impedance discontinuity models were not added to the schematic. A simulation was run on the circuit in Figure 11 with LINC2 abrupt impedance step models added between each microstrip. With the abrupt change in microstrip width modeled, the maximum change in S21 was 0.4 dB at any point within the operating band. Thus it was deemed unnecessary to include these discontinuity models for this circuit at this frequency band. It would also be a good idea to check out the effect of complete parasitic models for the few lumped components used in the design. However, particular attention was given to modeling the ground via structure for the FET's source leads because the circuit is most sensitive to grounding in this area.

Features of the new LINC2 optimizer were also presented. Figures 9 and 10 show how user defined equations can be included in the LINC2 optimization process. This article demonstrated the power of this new capability to control the physical size of the circuit in addition to optimizing electrical circuit responses. It is a powerful new capability that the same optimizer that optimizes RF circuit performance can also be directed to restrain or reduce physical size, seemingly independent from any direct relationship to electrical performance.

The LINC2 Software Suite

LINC2 is a high performance RF and microwave design and simulation program from ACS. In addition to schematic based circuit simulation, optimization and statistical yield analysis, LINC2 Pro includes many value-added features for automating design tasks, including circuit synthesis.

LINC2 offers exact circuit synthesis, schematic capture, circuit simulation, circuit optimization and yield analysis in a single affordable design environment. More information about LINC2 and links to other related articles can be found on the ACS web site at www.appliedmicrowave.com.

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